

HD14040B

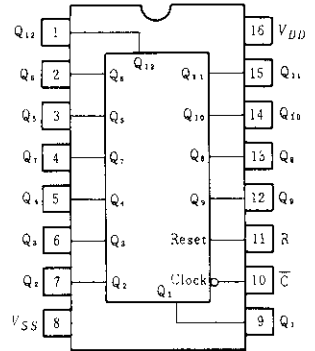
12-bit Binary Counter

The HD14040B 12-stages binary counter is designed with an input wave shaping circuit and 12-stages of ripple-carry binary counter. The device advances the count on the negative-going edge of the clock pulse. Applications include time delay circuits, counter controls, and frequency-dividing circuits.

FEATURES

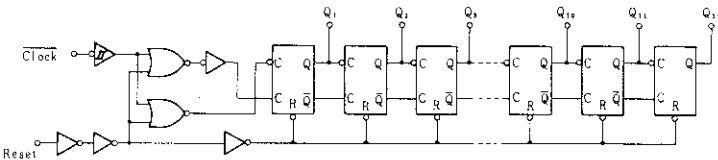
- Fully Static Operation
- Quiescent Current = 5nA/pkg typ. @5V
- Supply Voltage Range = 3 to 18V
- Capable of Driving One Low-power Schottky TTL Load Over the Rated Temperature Range
- Common Reset Line
- 13MHz Typical Counting Rate @15V
- Pin-for-Pin Replacement for CD4040B and MC14040B

PIN ARRANGEMENT



(Top View)

LOGIC DIAGRAM

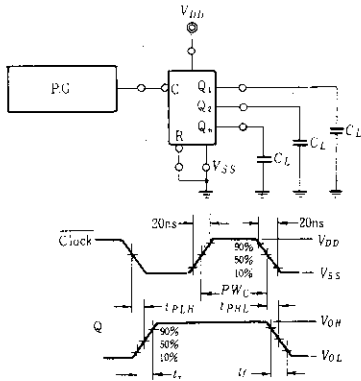


TRUTH TABLE

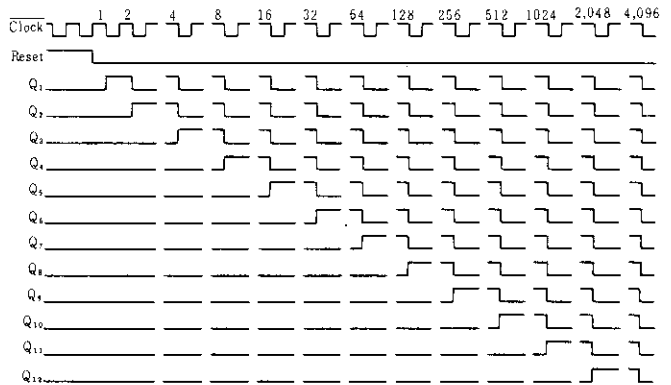
\bar{C}	Reset	Outputs State
	0	No Change
	0	Advance to next state
x	1	All Outputs are low

x = Don't Care

SWITCHING TIME TEST CIRCUIT



TIMING DIAGRAM

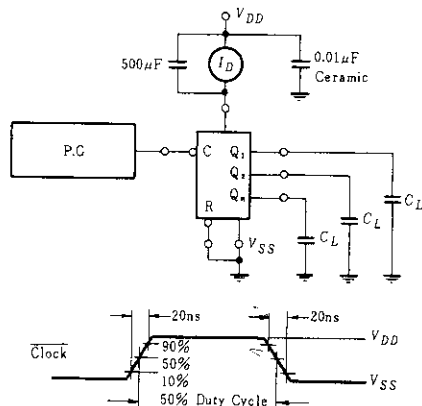


ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	$V_{DD}(V)$	Test Conditions	-40°C		25°C			85°C		Unit
				min	max	min	typ	max	min	max	
Output Voltage	V_{OL}	5.0	$V_{in} = V_{DD}$ or 0	-	0.05	-	0	0.05	-	0.05	V
		10		-	0.05	-	0	0.05	-	0.05	
		15		-	0.05	-	0	0.05	-	0.05	
	V_{OH}	5.0	$V_{in} = 0$ or V_{DD}	4.95	-	4.95	5.0	-	4.95	-	V
		10		9.95	-	9.95	10	-	9.95	-	
		15		14.95	-	14.95	15	-	14.95	-	
Input Voltage	V_{IL}	5.0	$V_{out} = 4.5$ or $0.5V$	-	1.5	-	2.25	1.5	-	1.5	V
		10	$V_{out} = 9.0$ or $1.0V$	-	3.0	-	4.50	3.0	-	3.0	
		15	$V_{out} = 13.5$ or $1.5V$	-	4.0	-	6.75	4.0	-	4.0	
	V_{IH}	5.0	$V_{out} = 0.5$ or $4.5V$	3.5	-	3.5	2.75	-	3.5	-	V
		10	$V_{out} = 1.0$ or $9.0V$	7.0	-	7.0	5.50	-	7.0	-	
		15	$V_{out} = 1.5$ or $13.5V$	11.0	-	11.0	8.25	-	11.0	-	
Output Drive Current	I_{OH}	5.0	$V_{OH} = 2.5V$	-1.0	-	-0.8	-1.7	-	-0.6	-	mA
		5.0	$V_{OH} = 4.6V$	-0.2	-	-0.16	-0.36	-	-0.12	-	
		10	$V_{OH} = 9.5V$	-0.5	-	-0.4	-0.9	-	-0.3	-	
		15	$V_{OH} = 13.5V$	-1.4	-	-1.2	-3.5	-	-1.0	-	
	I_{OL}	5.0	$V_{OL} = 0.4V$	0.52	-	0.44	0.88	-	0.36	-	mA
		10	$V_{OL} = 0.5V$	1.3	-	1.1	2.25	-	0.9	-	
15		$V_{OL} = 1.5V$	3.6	-	3.0	8.8	-	2.4	-		
Input Current	I_{in}	15		-	± 0.3	-	± 0.0001	± 0.3	-	± 1.0	μA
Input Capacitance	C_{in}	-	$V_{in} = 0$	-	-	-	5.0	7.5	-	-	pF
Quiescent Current	I_{DD}	5.0	Zero Signal, per Package	-	20	-	0.005	20	-	150	μA
		10		-	40	-	0.010	40	-	300	
		15		-	80	-	0.015	80	-	600	
Total Supply Current*	I_T	5.0	Dynamic + I_{DD} , $C_L = 50pF$	-	-	-	0.42	-	-	-	μA
		10	$f = 1kHz$	-	-	-	0.85	-	-	-	
		15	per Gate	-	-	-	1.43	-	-	-	

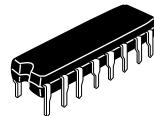
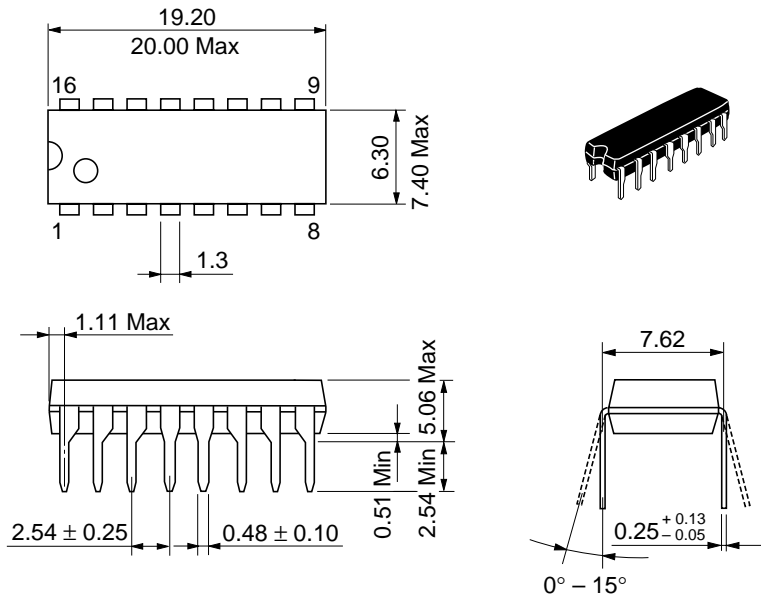
* To calculate total supply current at frequency other than 1kHz.
 @ $V_{DD} = 5.0V$ $I_T = (0.42\mu A/kHz)f + I_{DD}$ @ $V_{DD} = 10V$ $I_T = (0.85\mu A/kHz)f + I_{DD}$ @ $V_{DD} = 15V$ $I_T = (1.43\mu A/kHz)f + I_{DD}$

POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

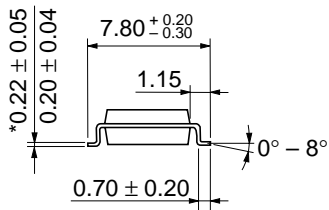
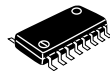
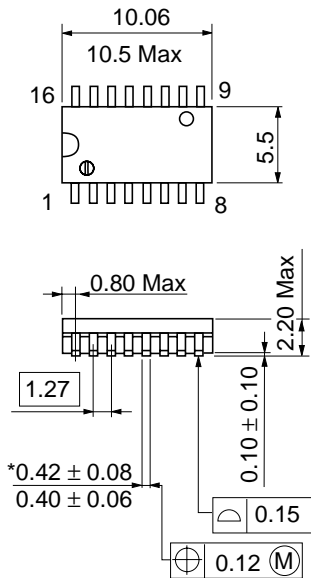


■SWITCHING CHARACTERISTICS ($C_L=50\text{pF}$, $T_a=25^\circ\text{C}$)

Characteristic	Symbol	V_{DD} (V)	min	typ	max	Unit	
Output Rise Time	t_r	5.0	—	180	400	ns	
		10	—	90	200		
		15	—	65	160		
Output Fall Time	t_f	5.0	—	100	200	ns	
		10	—	50	100		
		15	—	37	80		
Propagation Delay Time	Clock-to-Q ₁	t_{PLH}	5.0	—	400	1050	ns
			10	—	170	420	
			15	—	120	320	
	Clock-to-Q ₁₂	t_{PHL}	5.0	—	2.5	7.5	μs
			10	—	0.9	2.7	
			15	—	0.5	2.1	
	Reset-to-Qn	t_{PHL}	5.0	—	570	1620	ns
			10	—	215	600	
			15	—	170	450	
Clock Pulse Width	PW_C	5.0	385	140	—	ns	
		10	150	55	—		
		15	115	38	—		
Clock Frequency	PRF	5.0	—	3.5	1.5	MHz	
		10	—	9.0	3.5		
		15	—	13	4.5		
Clock Pulse Rise and Fall Time	t_r, t_f	5.0	No Limit				
		10					
		15					
Reset Pulse Width	PW_R	5.0	960	320	—	ns	
		10	360	120	—		
		15	270	80	—		

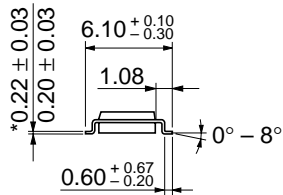
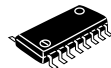
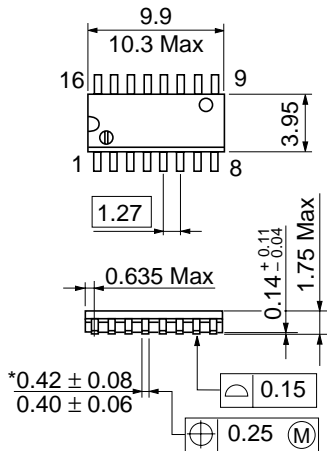


Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g



*Dimension including the plating thickness
 Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

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